# TS5USBC402 Dual 2:1 USB 2.0 Mux/DeMux or Single Ended Cross Switch with 20-V Overvoltage Protection

## 1 Features

- Supply Range 2.3 V to 5.5 V
- Differential 2:1 or 1:2 Switch/Multiplexer or Flexible Dual Single Ended Cross Switch
- 0-V to 20-V Overvoltage Protection (OVP) on Common Pins
- Powered Off Protection When $V_{CC}$ = 0 V
- Low $R_{ON}$ of 9 Ω Maximum
- BW of 1.2 GHz Typical
- $C_{ON}$ of 4.5 pF Typical
- Low Power Disable Mode
- 1.8-V Compatible Logic Inputs
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (HBM)
- TS5USBC402: Standard Temperature Range of 0°C to 70°C
- TS5USBC402I: Industrial Temperature Range of -40°C to 85°C
- Small DSBGA Package

## 2 Applications

- Mobile
- PC/Notebook
- Tablet
- Anywhere a USB Type-C™ or Micro-B Connector is Used

## 3 Description

The TS5USBC402 is a bidirectional low-power dual port, high-speed, USB 2.0 analog switch with integrated protection for USB Type-C™ systems. The device is configured as a dual 2:1 or 1:2 switch and is optimized for handling the USB 2.0 D+/- lines in a USB Type-C™ systems.

The TS5USBC402 protection on the I/O pins can tolerate up to 20 V with automatic shutoff circuitry to protect system components behind the switch.

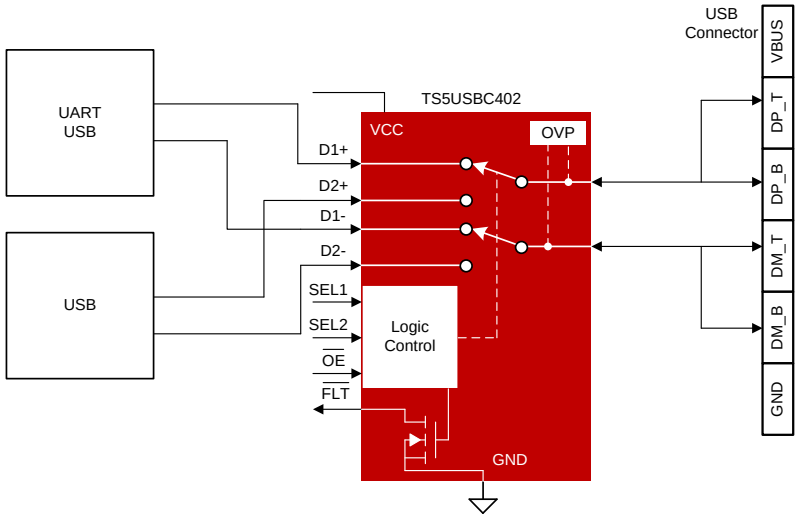
The TS5USBC402 comes in a small 12 pin DSBGA package making it a perfect candidate for mobile and space constrained applications.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TS5USBC402<br>TS5USBC402I | DSBGA (12) | 1.582 mm × 1.182 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**



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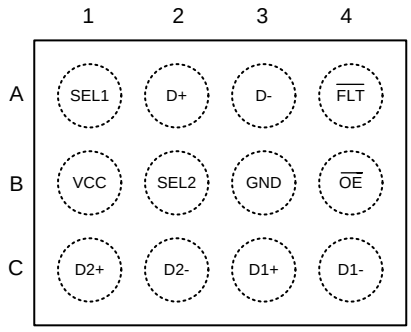
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (September 2017) to Revision A | Page |
|---|---|
| • Added $I_{CC}$ Active supply current and Supply current during OVP condition to the E*lectrical Specification* table | 4 |

# 5 Pin Configuration and Functions

**YFP Package**
**12-Pin DSBGA**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SEL1 | A1 | I | Switch select1 (Active high) |
| D+ | A2 | I/O | Data switch input (Differential +) |
| D– | A3 | I/O | Data switch input (Differential –) |
| $\overline{FLT}$ | A4 | O | Fault indicator output pin (Active low) - open drain |
| VCC | B1 | PWR | Supply Voltage |
| SEL2 | B2 | I | Switch select2 (Active high) |
| GND | B3 | GND | Ground |
| $\overline{OE}$ | B4 | I | Output enable (Active low) |
| D2+ | C1 | I/O | Data switch output 2 (Differential +) |
| D2– | C2 | I/O | Data switch output 2 (Differential -) |
| D1+ | C3 | I/O | Data switch output 1 (Differential +) |
| D1– | C4 | I/O | Data switch output 1 (Differential -) |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage(3) | | –0.5 | 6 | V |
| $V_{I/O}$ | Input/Output DC voltage (D+, D-)(3) | | –0.5 | 20 | V |
| $V_{I/O}$ | Input/Output DC voltage (D1+/D1-, D2+/D2-) (3) | | –0.5 | 6 | V |
| $V_I$ | Digital input voltage (SEL1, SEL2, $\overline{OE}$) | | –0.5 | 6 | V |
| $V_O$ | Digital output voltage ($\overline{FLT}$) | | –0.5 | 6 | V |
| $I_K$ | Input-output port diode current (D+, D-, D1+, D1-, D2+, D2-) | $V_{IN} < 0$ | –50 | | mA |
| $I_{IK}$ | Digital logic input clamp current (SEL1, SEL2, $\overline{OE}$) (3) | $V_I < 0$ | –50 | | mA |
| $I_{CC}$ | Continuous current through VCC | | | 100 | mA |
| $I_{GND}$ | Continuous current through GND | | –100 | | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.3 | 5.5 | V |
| $V_{I/O\ (D+,\ D-)}$ | Analog input/output voltage | 0 | 18 | V |
| $V_{I/O\ (D1,\ D1-,\ D2+,\ D2-)}$ | | 0 | 3.6 | V |
| $V_I$ | Digital input voltage (SEL1, SEL2, $\overline{OE}$) | 0 | 5.5 | V |
| $V_O$ | Digital output voltage ($\overline{FLT}$) | 0 | 5.5 | V |
| $I_{I/O\ (D+,\ D-,\ D1+,\ D1-,\ D2+,\ D2-)}$ | Analog input/output port continuous current | -50 | 50 | mA |
| $I_{OL}$ | Digital output current | | 3 | mA |
| $T_A$ | Operating free-air temperature (TS5USBC402) Standard | 0 | 70 | ºC |
| $T_A$ | Operating free-air temperature (TS5USBC402I) Industrial | –40 | 85 | ºC |
| $T_J$ | Junction temperature | –40 | 125 | ºC |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TS5USBC402 YFP 12 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 91.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 22.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 23.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

$T_A$ = –40°C to +85°C (Industrial), TA = 0℃ to 70℃ (Standard), $V_{CC}$ = 2.3 V to 5.5 V, GND = 0V, Typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $V_{CC}$ | Power supply voltage | | 2.3 | | 5.5 | V |
| $I_{CC}$ | Active supply current | $\overline{OE}$ = 0 V<br>SEL1, SEL2 = 0 V, 1.8 V or $V_{CC}$<br>0 V < $V_{I/O}$ < 3.6 V | | 72 | 100 | µA |
| | Supply current during OVP condition | $\overline{OE}$ = 0 V<br>SEL1, SEL2 = 0 V, 1.8 V or $V_{CC}$<br>$V_{I/O}$ > $V_{POS\_THLD}$ | | 80 | 120 | µA |
| $I_{CC\_PD}$ | Standby powered down supply current | $\overline{OE}$ = 1.8 V or $V_{CC}$<br>SEL1 = 0 V, 1.8 V, or VCC<br>SEL2 = 0 V, 1.8 V, or VCC | | 2.2 | 10 | µA |
| **DC Characteristics** | | | | | | |
| $R_{ON}$ | ON-state resistance | $V_{I/O}$ = 0.4 V<br>$I_{SINK}$ = 8 mA<br>Refer to ON-State Resistance Figure | | 5.6 | 9 | Ω |
| $\Delta R_{ON}$ | ON-state resistance match between channels | $V_{I/O}$ = 0.4 V<br>$I_{SINK}$ = 8 mA<br>Refer to ON-State Resistance Figure | | 0.07 | 0.3 | Ω |
| $R_{ON\ (FLAT)}$ | ON-state resistance flatness | $V_{I/O}$ = 0 V to 0.4 V<br>$I_{SINK}$ = 8 mA<br>Refer to ON-State Resistance Figure | | 0.07 | 0.4 | Ω |
| $I_{OFF}$ | I/O pin OFF leakage current | $V_{D\pm}$ = 0 V or 3.6 V<br>$V_{CC}$ = 2.3 V to 5.5 V<br>$V_{D1\pm}$or $V_{D2+/-}$ = 3.6 V or 0 V<br>Refer to Off Leakage Figure | -1 | 1.2 | 6 | µA |
| | | $V_{D\pm}$ = 0 V or 20 V<br>$V_{CC}$ = 2.3 V to 5.5 V<br>$V_{D1\pm}$ or $V_{D2+/-}$ = 0 V<br>Refer to Off Leakage Figure | -1 | 165 | 200 | µA |
| $I_{ON}$ | ON leakage current | $V_{D\pm}$ = 0 V or 3.6 V<br>$V_{D1\pm}$ and $V_{D2+/-}$ = high-Z<br>Refer to On Leakage Figure | -1 | 1.2 | 6 | µA |
| **Digital Characteristics** | | | | | | |
| $V_{IH}$ | Input logic high | SEL1, SEL2, $\overline{OE}$ | 1.4 | | | V |
| $V_{IL}$ | Input logic low | SEL1, SEL2, $\overline{OE}$ | | | 0.5 | V |
| $V_{OL}$ | Output logic low | $\overline{FLT}$<br>$I_{OL}$ = 3 mA | | | 0.4 | V |
| $I_{IH}$ | Input high leakage current | SEL1, SEL2, $\overline{OE}$ = 1.8 V, $V_{CC}$ | -1 | 1 | 5 | µA |
| $I_{IL}$ | Input low leakage current | SEL1, SEL2, $\overline{OE}$ = 0 V | -1 | ±0.2 | 5 | µA |

## Electrical Characteristics (continued)

$T_A$ = –40°C to +85°C (Industrial), TA = 0℃ to 70℃ (Standard), $V_{CC}$ = 2.3 V to 5.5 V, GND = 0V, Typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{PD}$ | Internal pull-down resistor on digital input pins | | | 6 | | MΩ |
| $C_I$ | Digital input capacitance | SEL1, SEL2 = 0 V, 1.8 V or VCC<br>f = 1 MHz | | 3.4 | | pF |
| **Protection** | | | | | | |
| $V_{OVP\_TH}$ | OVP positive threshold | | 4.5 | 4.8 | 5.2 | V |
| $V_{OVP\_HYST}$ | OVP threshold hysteresis | | 75 | 230 | 425 | mV |
| $V_{CLAMP\_V}$ | Maximum voltage to appear on D1± and D2± pins during OVP scenario | $V_{D±}$ = 0 to 18 V<br>$t_{RISE}$ and $t_{FALL}$(10% to 90 %) = 100 ns<br>$R_L$ = Open<br>Switch on or off<br>$\overline{OE}$ = 0 V | 0 | | 9.6 | V |
| | | $V_{D±}$ = 0 to 18 V<br>$t_{RISE}$ and $t_{FALL}$(10% to 90 %) = 100 ns<br>$R_L$ = 50Ω<br>Switch on or off<br>$\overline{OE}$ = 0 V | 0 | | 9.0 | V |
| $t_{EN\_OVP}$ | OVP enable time | $R_{PU}$ = 10 kΩ to VCC ($\overline{FLT}$)<br>$C_L$ = 35 pF<br>Refer to OVP Timing Diagram Figure | | 0.6 | 3 | µs |
| $t_{REC\_OVP}$ | OVP recovery time | $R_{PU}$ = 10 kΩ to VCC ($\overline{FLT}$)<br>$C_L$ = 35 pF<br>Refer to OVP Timing Diagram Figure | | 1.5 | 5 | µs |

## 6.6 Dynamic Characteristics

$T_A$ = –40°C to +85°C (Industrial), TA = 0℃ to 70℃ (Standard), $V_{CC}$ = 2.3 V to 5.5V, GND = 0V, Typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C, (unless otherwise noted)

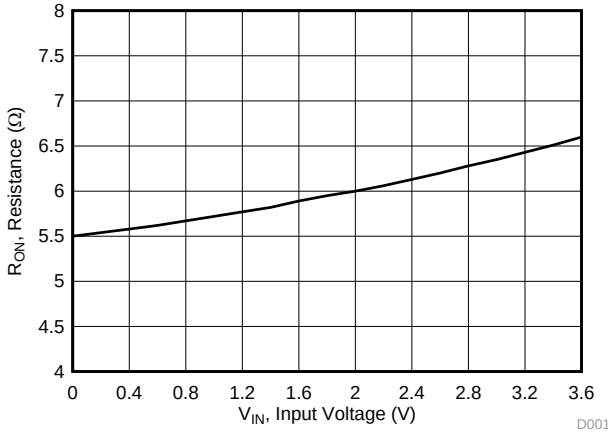
| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{OFF}$ | D+, D- off capacitance | $\overline{V_{D+/-}}$ = 0 or 3.3 V, $\overline{OE}$ = $V_{CC}$ f = 240 MHz | Switch OFF | 1.2 | 3.5 | 6.2 | pF |
| | D1+, D1-, D2+, D2- off capacitance | $\overline{V_{D+/-}}$ = 0 or 3.3 V, $\overline{OE}$ = $V_{CC}$ or $\overline{OE}$ = 0V with SEL1, SEL2 (switch not selected) f = 240 MHz | Switch OFF or not selected | 1.2 | 3.5 | 6.2 | pF |
| $C_{ON}$ | IO pins ON capacitance | $V_{D+/-}$ = 0 or 3.3 V, f = 240 MHz | Switch ON | 1.4 | 4.5 | 6.2 | pF |
| $O_{ISO}$ | Differential off isolation | RL = 50 Ω CL = 5 pF f = 100 kHz Refer to Off Isolation Figure | Switch OFF | | -90 | | dB |
| | | RL = 50 Ω CL = 5 pF f = 240 MHz Refer to Off Isolation Figure | Switch OFF | | -22 | | dB |
| $X_{TALK}$ | Channel to Channel crosstalk | RL = 50 Ω CL = 5 pF f = 100 kHz Refer to Crosstalk Figure | Switch ON | | -90 | | dB |
| BW | Bandwidth | RL = 50 Ω; Refer to BW and Insertion Loss Figure | Switch ON | | 1.2 | | GHz |
| $I_{LOSS}$ | Insertion loss | RL = 50 Ω f = 240 MHz; Refer to BW and Insertion Loss Figure | Switch ON | | -0.7 | | dB |

## 6.7 Timing Requirements

$T_A$ = –40°C to +85°C (Industrial), TA = 0℃ to 70℃ (Standard), $V_{CC}$ = 2.3 V to 5.5V, GND = 0V, Typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{switch}$ | Switching time between channels (SEL1, SEL2 to output) | $V_{D+/-}$ = 0.8 V Refer to Tswitch Timing Figure | $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_{CC}$ = 2.3 V to 5.5 V | | 0.45 | 1.2 | µs |
| $t_{on}$ | Device turn on time ($\overline{OE}$ to output) | $V_{D+/-}$ = 0.8 V Refer to Ton and Toff Figure | | | 100 | 250 | µs |
| $t_{off}$ | Device turn off time ($\overline{OE}$ to output) | $V_{D+/-}$ = 0.8 V Refer to Ton and Toff Figure | | | 0.35 | 1 | µs |
| $t_{SK(P)}$ | Skew of opposite transitions of same output (between D+ and D-) | $V_{D+/-}$ = 0.4 V Refer to Tsk Figure | $R_L$ = 50 Ω, $C_L$ = 1 pF, $V_{CC}$ = 2.3 V to 5.5 V | | 9 | 50 | ps |
| $t_{pd}$ | Propagation delay | $V_{D+/-}$ = 0.4 V Refer to Tpd Figure | $R_L$ = 50 Ω, $C_L$ = 5 pF, $V_{CC}$ = 2.3 V to 5.5 V | | 130 | 180 | ps |

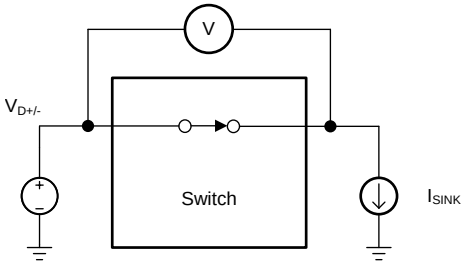
## 6.8 Typical Characteristics




$V_{CC}$ = 3.3 V $T_A$ = 25°C

**Figure 1. ON-Resistance vs Input Voltage**

# 7 Parameter Measurement Information




Channel ON, $R_{ON} = V/I_{SINK}$

**Figure 2. ON-State Resistance ($R_{ON}$)**

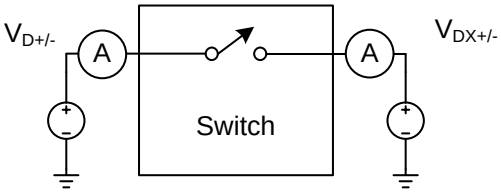



**Figure 3. Off Leakage**

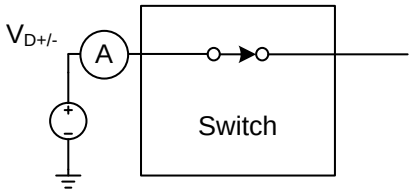
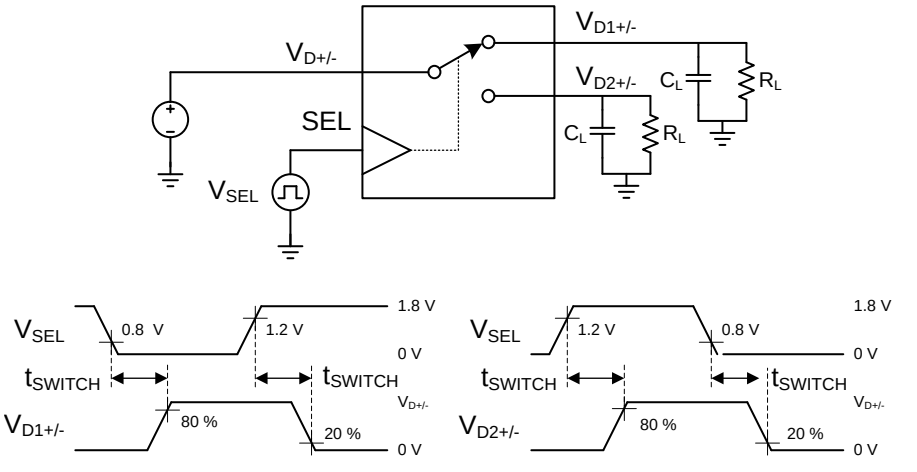



**Figure 4. On Leakage**



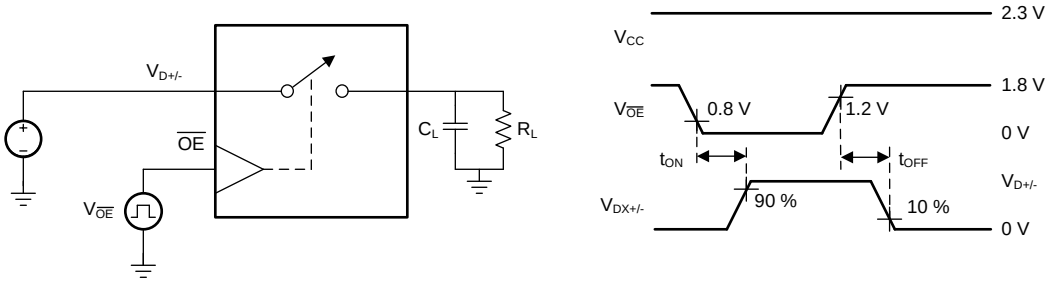



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 500 ps, $t_f$ < 500 ps.

(2) $C_L$ includes probe and jig capacitance.

**Figure 5. $t_{SWITCH}$ Timing**

## Parameter Measurement Information (continued)






(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 500 ps, $t_f$ < 500 ps.

(2) $C_L$ includes probe and jig capacitance.

**Figure 6. $t_{ON}$, $t_{OFF}$ for $\overline{OE}$**

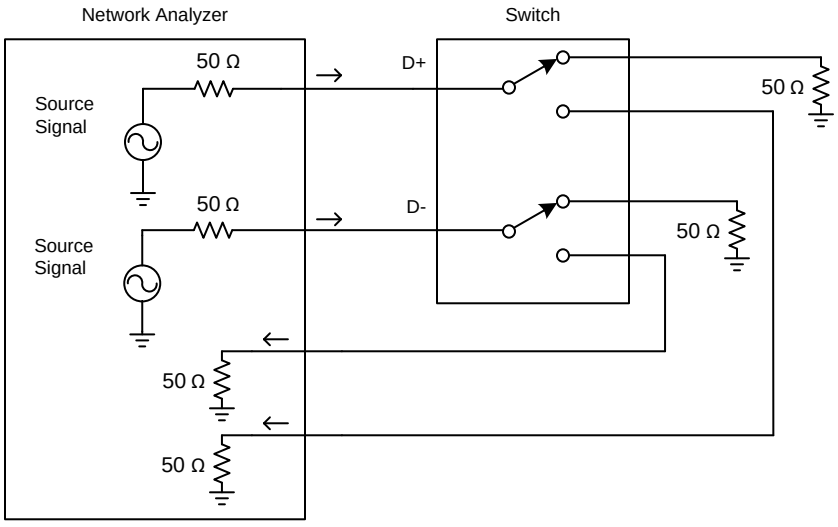





**Figure 7. Off Isolation**

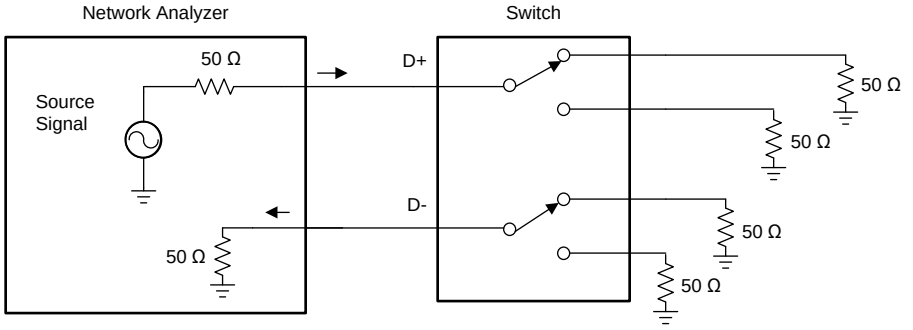





**Figure 8. Cross Talk**

## Parameter Measurement Information (continued)

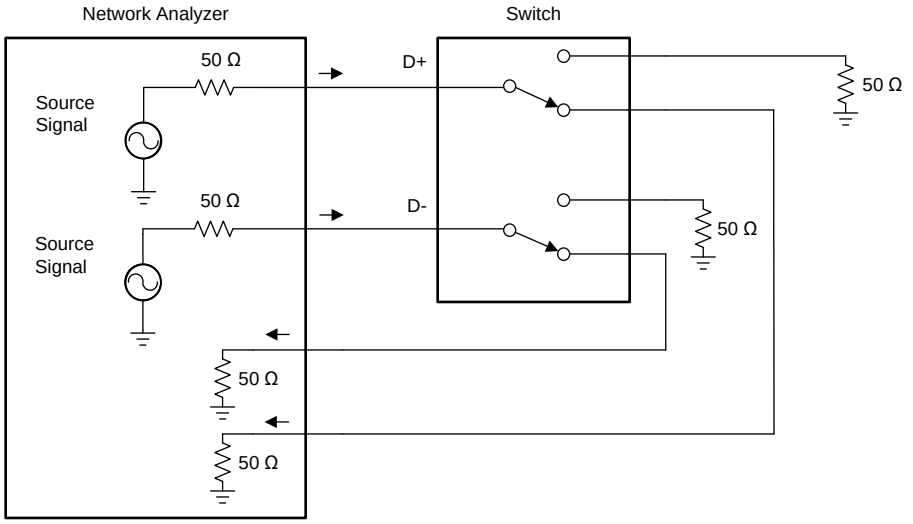





**Figure 9. BW and Insertion Loss**

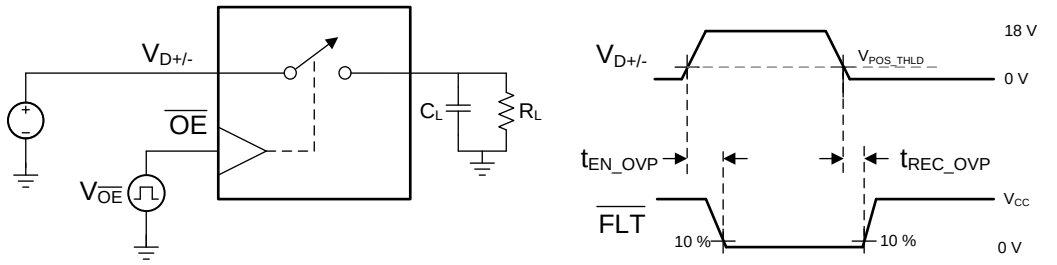
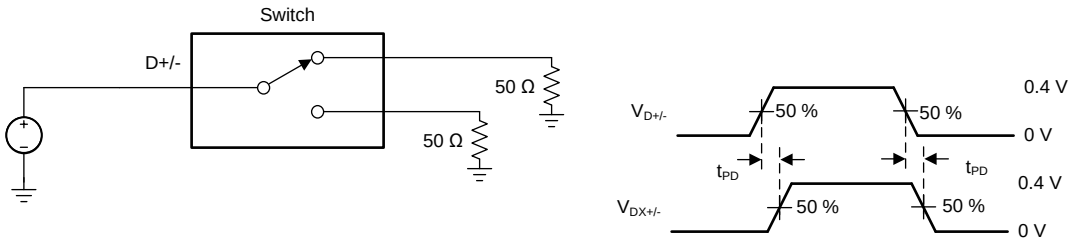





**Figure 10. $t_{EN\_OVP}$ and $t_{DIS\_OVP}$ Timing Diagram**



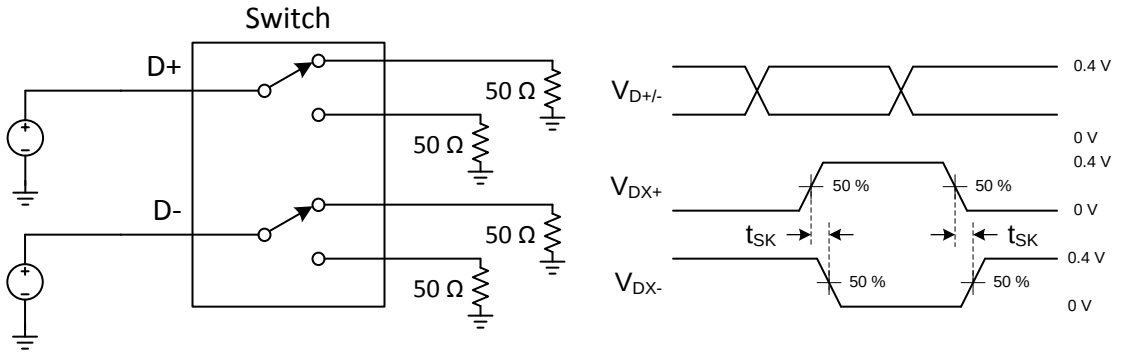



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 500 ps, $t_f$ < 500 ps.

(2) $C_L$ includes probe and jig capacitance.

**Figure 11. $t_{PD}$**

## Parameter Measurement Information (continued)






(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 500 ps, $t_f$ < 500 ps.

(2) $C_L$ includes probe and jig capacitance.

**Figure 12. $t_{SK}$**

# 8 Detailed Description

## 8.1 Overview

The TS5USBC402 is a bidirectional low-power dual port, high-speed, USB 2.0 analog switch with integrated protection for USB Type-C systems. The device is configured as a dual 2:1 or 1:2 switch and is optimized for handling the USB 2.0 D+/- lines in a USB Type-C system as shown in Figure 13.

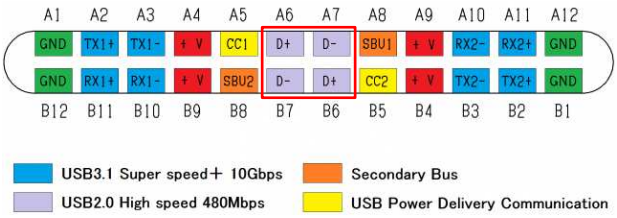
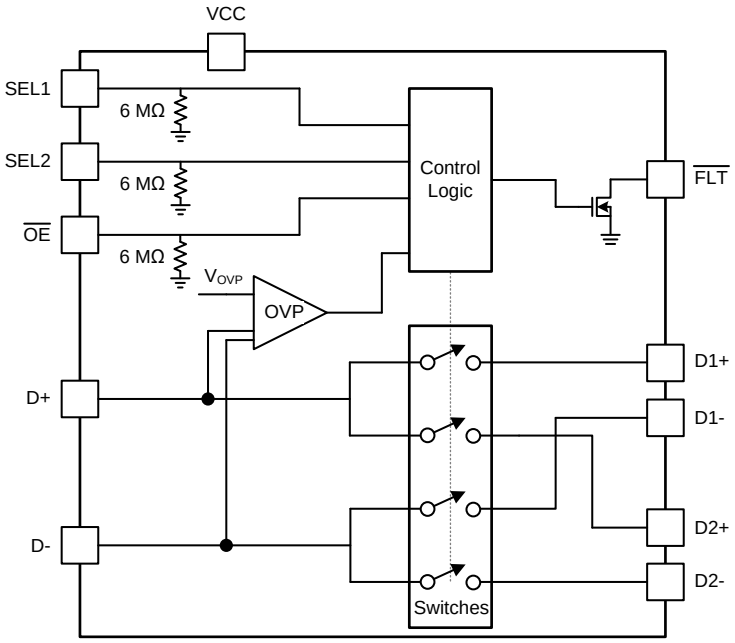



**Figure 13. USB Type-C Connector Pinout**

The TS5USBC402 also works in traditional USB systems that need protection from fault conditions such as automotive and applications that require higher voltage charging. The device maintains excellent signal integrity through the optimization of both $R_{ON}$ and BW while protecting the system with 0 V to 20 V OVP protection. The OVP implementation is designed to protect sensitive system components behind the switch that cannot survive a fault condition where VBUS is shorted the D+ and D- pins on the connector.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Powered-off Protection

When the TS5USBC402 is powered off the I/Os of the device remain in a high-Z state. The crosstalk, off-isolation, and leakage remain within the *Electrical Specifications*.

This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

### 8.3.2 Overvoltage Protection

The OVP of the TS5USBC402 is designed to protect the system from D+/- shorts to VBUS at the USB and USB Type-C connector. Figure 14 depicts a moisture short that would cause 20 V to appear on an existing USB solution that could pass through the device and damage components behind the device.

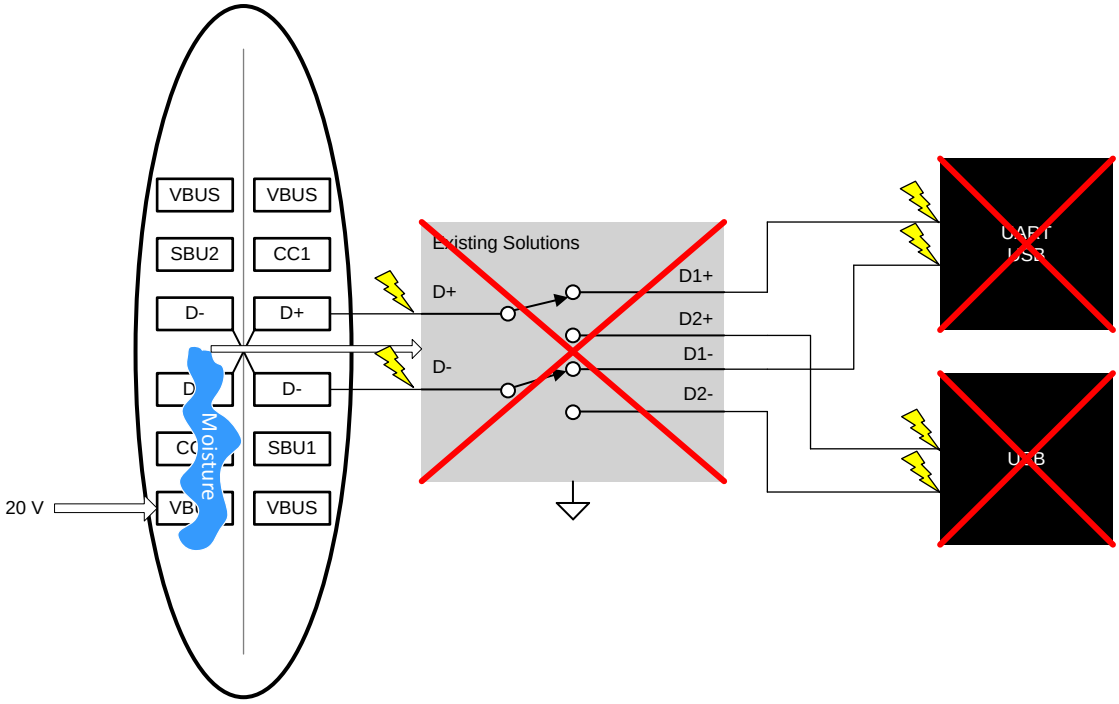





**Figure 14. Existing Solution Being Damaged by a Short, 20 V**

The TS5USBC402 will open the switches and protect the rest of the system by blocking the 20 V as depicted in Figure 15.

## Feature Description (continued)

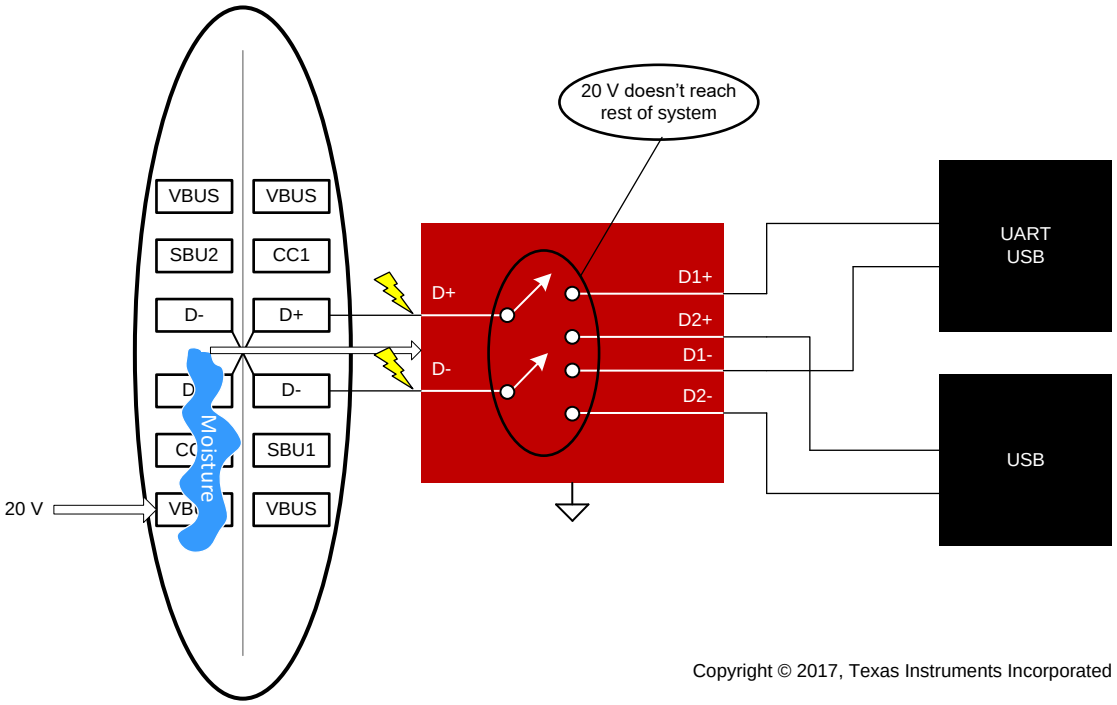





**Figure 15. Protecting During a 20-V Short**

Figure 16 is a waveform showing the voltage on the pins during an over-voltage scenario.

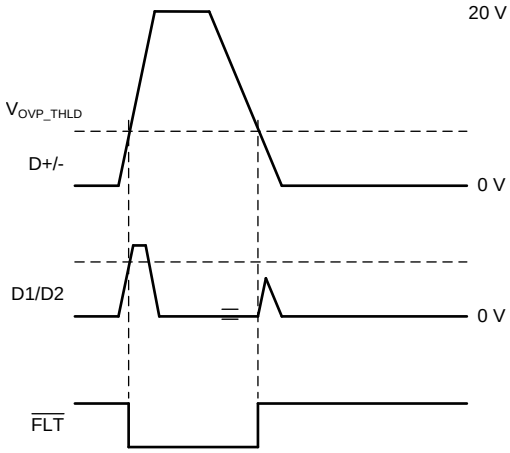



**Figure 16. Overvoltage Protection Waveform, 20 V**

## 8.4 Device Functional Modes

### 8.4.1 Pin Functions

**Table 1. Function Table**

| $\overline{OE}$ | SEL1 | SEL2 | D- Connection | D+ Connection |
|---|---|---|---|---|
| H | X | X | High-Z | High-Z |
| L | L | L | D- to D1- | D+ to D1+ |
| L | L | H | D- to D1- | D+ to D2+ |
| L | H | L | D- to D2- | D+ to D1+ |
| L | H | H | D- to D2- | D+ to D2+ |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os or need to route signals from a single USB connector. The TS5USBC402 solution can effectively expand the limited USB I/Os by switching between multiple USB buses to interface them to a single USB hub or controller or route signals from on connector to two different locations. With independent control of the two switches using SEL1 and SEL2, TS5USBC402 can be used to cross switch single ended signals.

## 9.2 Typical Application

TS5USBC402 USB/UART switch. The TS5USBC402 is used to switch signals between the USB path, which goes to the baseband or application processor, or the UART path, which goes to debug port. The TS5USBC402 has internal 6-MΩ pull-down resistors on SEL1, SEL2, and $\overline{OE}$. The pull-down on SEL1 and SEL2 pins ensure the D1+/D1- channel is selected by default. The pull-down on $\overline{OE}$ enables the switch when power is applied.

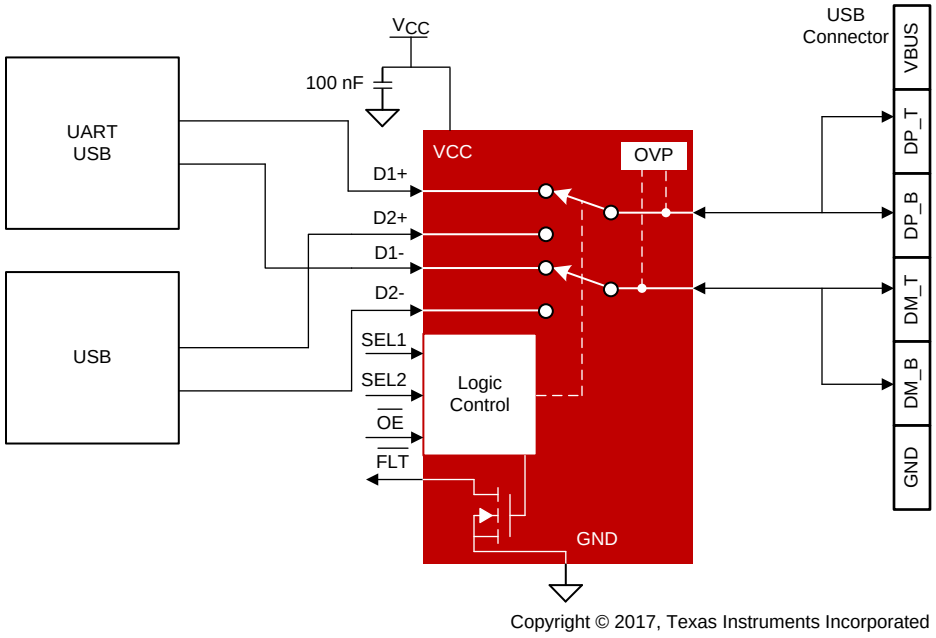





**Figure 17. Typical TS5USBC402 Application**

### 9.2.1 Design Requirements

Design requirements of USB 1.0,1.1, and 2.0 standards must be followed. The TS5USBC402 has internal 6-MΩ pulldown resistors on SEL1, SEL2, and $\overline{OE}$, so no external resistors are required on the logic pins. The internal pull-down resistor on SEL1 and SEL2 pins ensures the D1+ and D1- channels are selected by default. The internal pull-down resistor on $\overline{OE}$ enables the switch when power is applied to VCC.

### 9.2.2 Detailed Design Procedure

The TS5USBC402can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI does recommend a 100nF bypass capacitor placed close to TS5USBC402 VCC pin.

## Typical Application (continued)

### 9.2.3 Application Curves

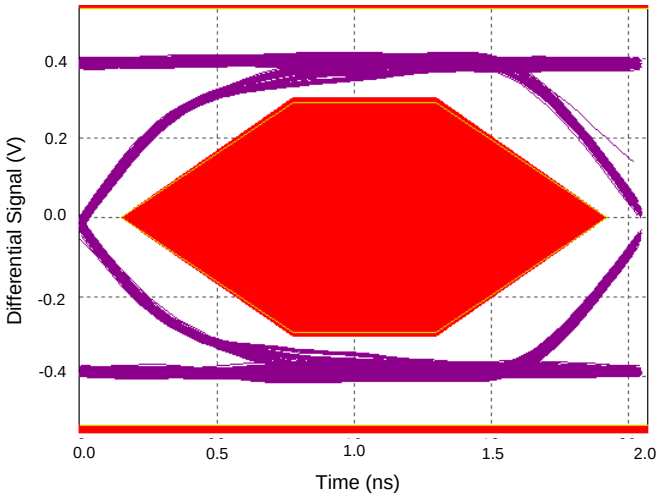



**Figure 18. High Speed Eye Diagram With TS5USBC402**

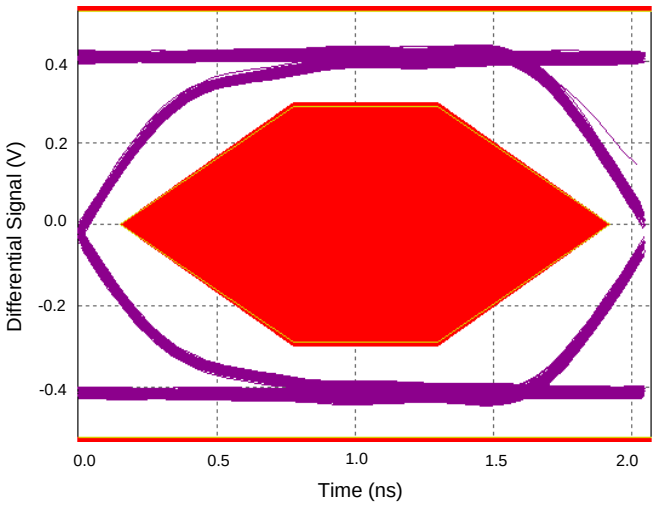



**Figure 19. High Speed Eye Diagram Without TS5USBC402**

## 10 Power Supply Recommendations

Power to the device is supplied through the VCC pin and must follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a 100nF bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

# 11 Layout

## 11.1 Layout Guidelines

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D± traces.
2. The high-speed D± must match and be no more than 4 inches long; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces must match the cable characteristic differential impedance for optimal performance.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
5. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
6. Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.
7. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
8. Avoid crossing over anti-etch, commonly found with plane splits.
9. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 20.

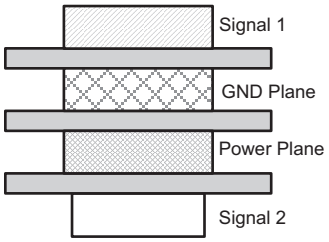



**Figure 20. Four-Layer Board Stack-Up**

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

## 11.2 Layout Example

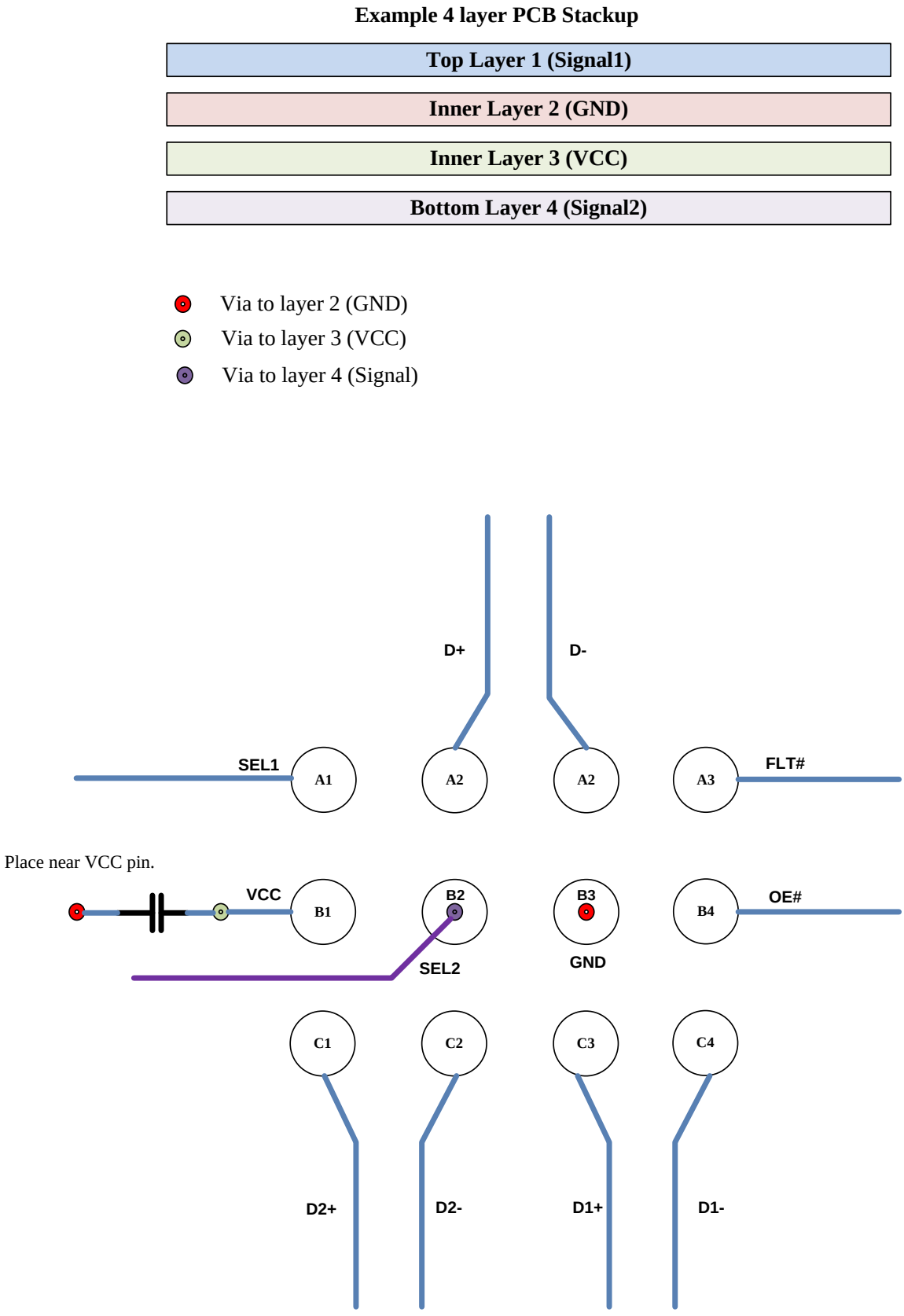



**Figure 21. Layout Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- *USB 2.0 Board Design and Layout Guidelines*
- *High-Speed Layout Guidelines Application Report*
- *High-Speed Interface Layout Guidelines*

## 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.3 Trademarks

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## 12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

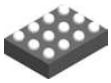
This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

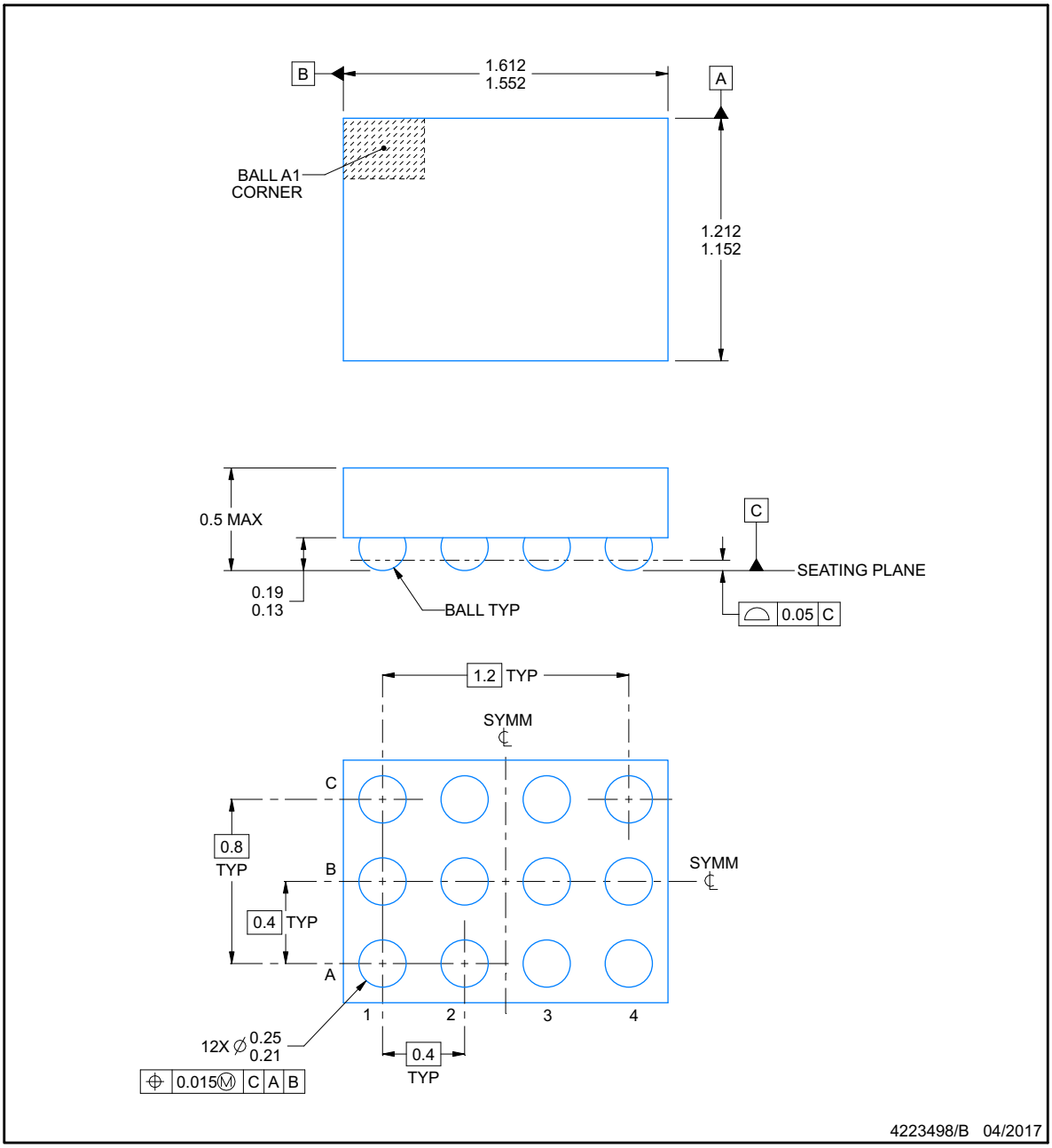
# PACKAGE OUTLINE

## YFP0012-C01



## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




NOTES:

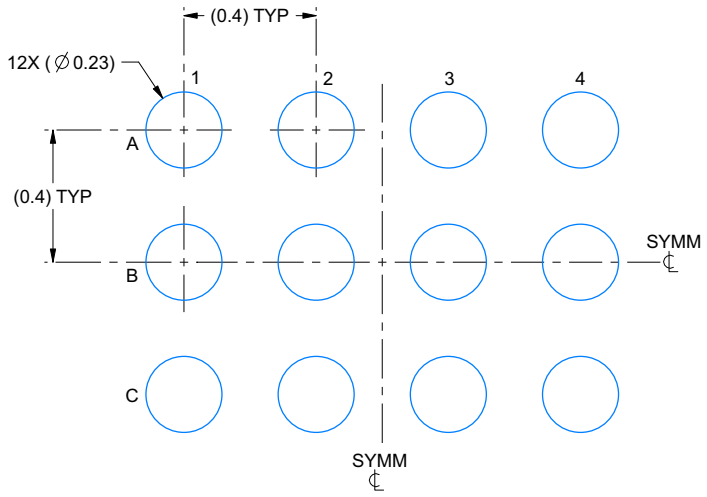
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

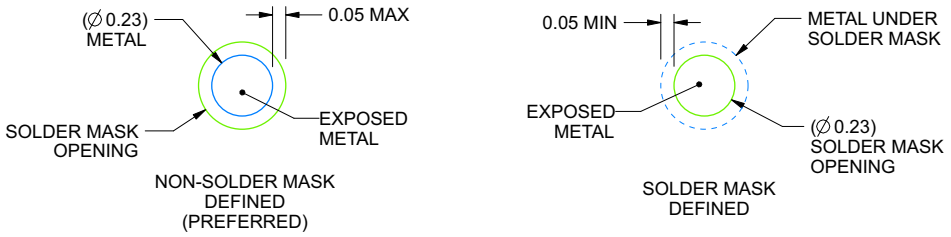
## YFP0012-C01

### DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X




SOLDER MASK DETAILS
NOT TO SCALE

4223498/B 04/2017

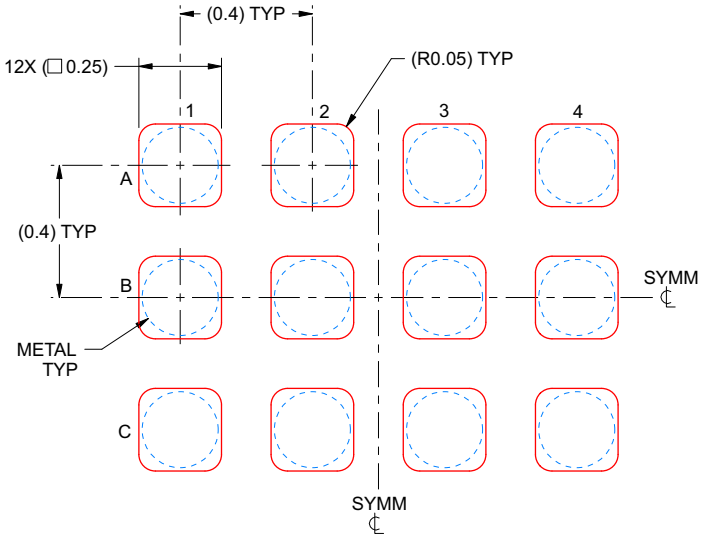
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

## EXAMPLE STENCIL DESIGN

**YFP0012-C01** — **DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223498/B 04/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TS5USBC402IYFPR | ACTIVE | DSBGA | YFP | 12 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | USB4 | Samples |
| TS5USBC402IYFPT | ACTIVE | DSBGA | YFP | 12 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | USB4 | Samples |
| TS5USBC402YFPR | ACTIVE | DSBGA | YFP | 12 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | 0 to 70 | USB4 | Samples |
| TS5USBC402YFPT | ACTIVE | DSBGA | YFP | 12 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | 0 to 70 | USB4 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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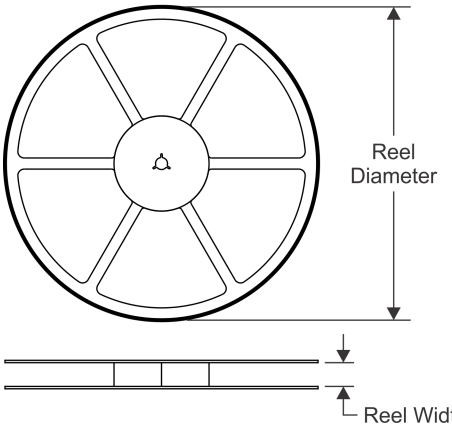
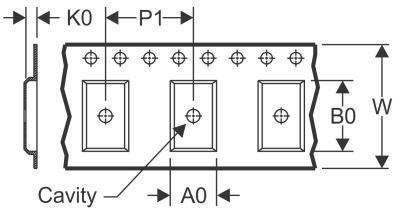
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

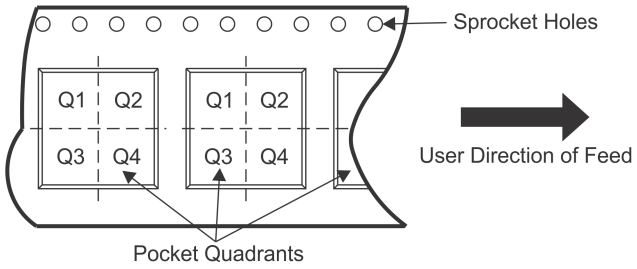



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

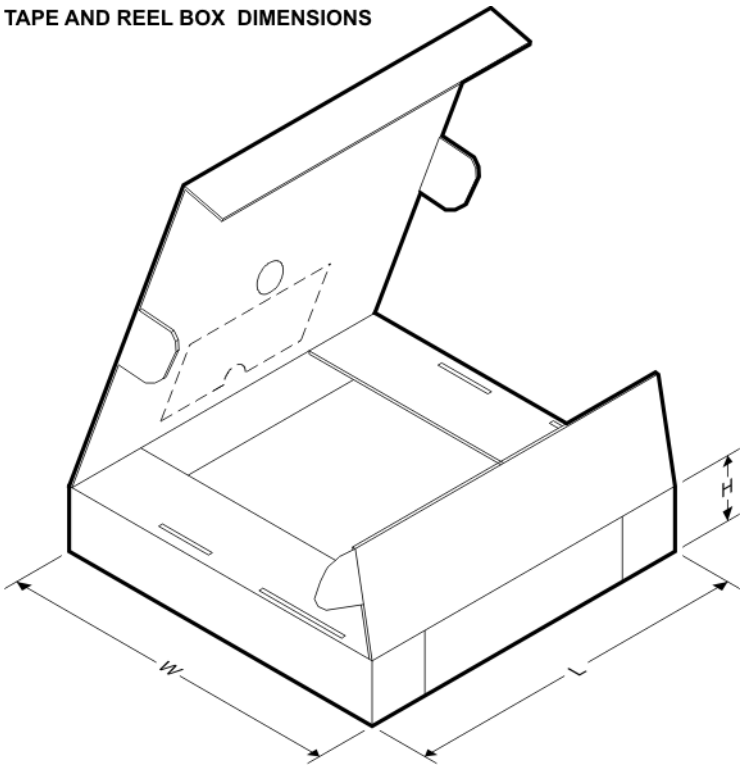
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TS5USBC402IYFPR | DSBGA | YFP | 12 | 3000 | 180.0 | 8.4 | 1.32 | 1.72 | 0.62 | 4.0 | 8.0 | Q2 |
| TS5USBC402IYFPT | DSBGA | YFP | 12 | 250 | 180.0 | 8.4 | 1.32 | 1.72 | 0.62 | 4.0 | 8.0 | Q2 |
| TS5USBC402YFPR | DSBGA | YFP | 12 | 3000 | 180.0 | 8.4 | 1.32 | 1.72 | 0.62 | 4.0 | 8.0 | Q2 |
| TS5USBC402YFPT | DSBGA | YFP | 12 | 250 | 180.0 | 8.4 | 1.32 | 1.72 | 0.62 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TS5USBC402IYFPR | DSBGA | YFP | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TS5USBC402IYFPT | DSBGA | YFP | 12 | 250 | 182.0 | 182.0 | 20.0 |
| TS5USBC402YFPR | DSBGA | YFP | 12 | 3000 | 182.0 | 182.0 | 20.0 |
| TS5USBC402YFPT | DSBGA | YFP | 12 | 250 | 182.0 | 182.0 | 20.0 |

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